AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 5, line 30, with the following:

The means of exchange generally consist of a serial link or a communication memory. In Fig. 5 such a communication memory has been represented. In this figure are seen the ~~DSP~~ main processor 5 (a DSP being selected in this embodiment) and the protocol processor 6 of the device of Fig. 2, the core 8 of the ~~DSP~~ main processor 5 is connected to the core 9 of the protocol processor 6 by synchronising circuit 10. The ~~DSP~~ main processor 5 further includes a program ROM memory 11 and a local RAM memory 12. The protocol processor 6 includes also, a program ROM memory 13 and a local RAM memory 14. The local RAM memories 12 and 14 of the ~~DSP~~ main processor 5 and of the protocol processor 6 are connected by a common DPRAM memory 15 with dual port. The synchronising of the processes P1 and P2 is performed by a test and set instruction TAS which, as indicated in Fig. 6, makes it possible to ensure that a single processor utilizes the DPRAM memory 15 (or memory zone) at any moment.

Please replace the paragraph beginning on page 6, line 8, with the following:

There also exist other process synchronising mechanisms. For example, with the TAS instruction of Fig. 6, the program P1 writes parameters for the program P2 to the DPRAM memory 15 ~~15~~.

Please replace the paragraph beginning on page 6, line 12, with the following:

Since the parameters are related, if P2 accesses the DPRAM memory 15 during modification by P1, there is a risk of error.

Please replace the paragraph beginning on page 6, line 15, with the following:

The program P1 tests, with the TAS instruction, whether the DPRAM memory 15 is available and generates an occupied signal. During modification of the parameters a,b,c, and d which are in the DPRAM memory 15, if the program P2 requests access to this memory zone, its TAS instruction returns an occupied signal to it. The program P1 frees the DPRAM memory 15 at the end of the access and the program P2 can then access the memory if it makes a new request.

Please replace the paragraph beginning on page 6, line 23, with the following:

As Fig. 5 shows, each processor has its own ROM program memory 11, 13 respectively, a local work memory 12, 14 and a processor core 8, 9. The synchronising means 10 and the DPRAM memory 15 are common to both processors.

Please replace the paragraph beginning on page 6, line 29, with the following:

The protocol processor 6 includes a processor ~~proper 16~~ core 9 connected to a program memory 17 by an address bus 18 and an instruction bus 19. It is connected at data-

stream level to a main processor 20 across a communication RAM memory 21 connected to each of the processors by a data bus 22, 23 and corresponding address bus 24, 25.

Please replace the paragraph beginning on page 6, line 35, with the following:

The ~~processor 16~~ core 9 can also be connected by data buses and selection and address buses 27, 28 to a hard-wired logic block 26 permitting the shaping of signals for a particular processing which it would be too costly to carry out by means of the ~~protocol processor 16~~ core 9. The logic block 26 is moreover connected to the ~~processor 16~~ core 9 by an interrupt line 29.

Please replace the paragraph beginning on page 7, line 4, with the following:

Fig. 8 shows in more detail the protocol processor 6 according to the invention.

Please replace the paragraph beginning on page 7, line 8, with the following:

A program part denoted with the general reference numeral 30 contains an incrementation register 31 which is incremented with each cycle except when an immediate value PMA is loaded by way of a bus 32. The register 31 generates the address of a memory in the shape of a program ~~33~~ which itself generates an instruction on a bus 34. The processor further comprises a decoder part denoted by the general reference numeral 35 which receives the code of the instruction from the program ROM memory ~~3~~13. This instruction is executed in two cycles in pipeline mode as the diagram of Fig. 9 shows.

Please replace the paragraph beginning on page 7, line 18, with the following:

During the cycle 1 indicated in this figure, the program ROM memory ~~3~~13 is read at the address PC1 of the incrementation register 31. At the end of the cycle, the instruction I1 delivered by the program ROM memory ~~3~~13 is decoded. During cycle 2, the operators of the instruction are read at the addresses specified by the code and the data part 36 which supplements the processor and which will subsequently be described executes the instruction. The result is stored at the address specified by the code of the instruction at the end of cycle 2.

Please replace the paragraph beginning on page 8, line 8, with the following:

This destination address is embodied in the diagram of Fig. 8 by a ~~dual-port~~ DPRAM memory [[44]]15 which is common to the protocol processor 6 and to the main processor~~ing unit CPU~~ 45 with which it is associated. The DPRAM memory 15[[44]] is connected to the main processor 5 ~~CPU 45~~ by means of a data and address bus 46, 47.

Please replace the paragraph beginning on page 8, line 36, with the following:

53 indicates a field @ + shift in which @ indicates that the registers X or B contain the address of access to the common DPRAM memory 15[[44]] of Fig. 8.